REMARKS

Claims 1-8 were examined and reported in the Office Action. Claims 1-8 were rejected. Applicants amend no claims, add no claims, and cancel no claims. Applicants respectfully request reconsideration of claims 1-8 in view of at least the following remarks.

I. Claims rejected under 35 U.S.C. § 103

Claims 1-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,001,685 to ("Kim") in combination with 5,683,939 to Schrantz et al. ("Schrantz").

Applicants respectfully disagree for at least the reason that the cited references cannot be properly combined. Kim describes a method of making a metal oxide semiconductor field effect transistor (MOSFET) having a structure capable of obtaining an increased alignment margin for a mask without any increase in the area of the semiconductor device by forming a contact plug electrically insulated from a gate electrode but in electrical contact with the drain, and a contact pad electrically insulated from the gate electrode but in electrical contact with the source. (See Abstract; and col. 3, lines 8-19) Specifically, the electrical insulation is provided by insulating materials, such as electrically insulating film 30, which may be a Boro-phospho-silicate glass (BPSG) (insulating film 30 corresponds to insulating film 10, see column 4 lines 61-62); and electrically insulating film 34 (insulating film 34 corresponds to insulating film 14, see column 5, lines 33-34). It is well known that BPSG is silicon dioxide with boron and phosphorous added to lower a temperature at which glass (Oxide) starts to flow from about 950°C for pure SiO_2 to about 500°C for BPSG. Although Kim specifies that insulation is with respect to electrically insulating features of a transistor, as described above, Kim makes no reference, teaching, or motivation related to thermal properties, temperature, heat, or insulation thereof. Finally, Kim teaches that the contact plug, contact pad, and insulating layers around the plug and pad are in the "lower portion" of the device (see col. 1, lines 32-36).

On the other hand, Schrantz describes fabricating multi-level interconnections with grown diamond insulation films and second level resistors for high temperature devices, such as galium arsenide-based circuits having a base, an emitter, and a collector (e.g., a bipolar transistor) (see Abstract; col. 1, lines 16-20; col. 2, lines 57-58). According to Schrantz, the high temperature circuits deviate from standard silicon structures because they are able to withstand higher temperature processing, such as deposition temperatures of CVD diamond, which is approximately 800°C which may be higher than for oxide deposition (e.g., higher than an oxide deposition which is at a temperature greater than the melting point of BPSG) (see col. 1, lines 23-27 and col. 2, lines 24-31).

Therefore, the references cannot be properly combined for at least the following reasons. First, there is no motivation in either reference for the combination. As noted above, Kim does not mention, teach, or suggest any material, structure, or process related to temperature, thermal consideration, heat, or dissipation thereof. Therefore, there is no motivation in Kim to add a thermally conducting material having a thermal conductivity greater than that of silicon dioxide, such as diamond. Similarly, Schrantz teaches a high temperature device capable of withstanding high temperature processing, such as deposition temperatures of CVD diamond "which may be higher than for oxide deposition." Thus, Schranz does not support that CVD diamond would be deposited on the MOSFET device of Kim, which has layers of oxide, silicon dioxide, and BPSG.

Second, combination of the Schranz diamond with the Kim device renders both references unsatisfactory for their intended purpose. It appears the MOSFET structure of Kim combined with Schranz could melt under the high temperature conditions of operation of the high temperature device of Schranz. Alternatively, the required temperature for the CVD deposition of the diamond layer of Schranz combined with Kim could melt the MOSFET structure of Kim during deposition. Specifically, the 800°C temperature (see Schrantz, col. 1, lines 28-32) used to grow the diamond layer in a mixture of hydrogen and methane, is greater than the melting of the BPSG layers of the Kim layer MOSFET by approximately 300°C. Thus, the BPSG electrically insulating films

of Kim could melt during deposition of the diamond layer of Schrantz on the MOSFET of Kim.

As a result, the Patent Office's motivation for combining the references because "the diamond film would be selected in accordance with the method of Kim in order to utilize the high thermal conductivity for dissipation of heat generated at local sources as taught by Schrantz," is completely unsupported. Kim neither teaches, suggests, requires, nor mentions dissipation of heat. Also, Schrantz specifies that its teachings are for high temperature processing which may be higher than for oxide deposition and for circuits able to withstand higher temperature operation than silicon devices (e.g., higher than for the MOSFET of Kim). Moreover, even if there were a motivation to combine the diamond film of Schrantz with Kim, deposition of the diamond film of Schrantz could melt the MOSFET device of Kim. Therefore, Applicants can only conclude that the motivation to combine the references includes knowledge gleaned only from Applicants' disclosure. As such, Applicants assert that the combination of Kim and Schrantz is the result of impermissible hindsight in accordance with MPEP § 2145.XA. Consequently, Applicants respectfully request that the Patent Office withdraw the rejection of independent claims 1 and 6 noted above for at least the above reasons.

Applicants submit that dependent claims 2-5 and 7-8, being dependent upon allowable base claims 1 and 6, are patentable over the cited references for at least the reasons explained above. Thus, Applicants respectfully request that the Patent Office withdraw the rejection of dependent claims 2-5 and 7-8 as being unpatentable over the cited references.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: 11/3/04

By: William Thomas Babbitt; Reg. No. 39,591

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on 11/3/04.

Nadya Gordon — 11/3/04
Nadya Gordon — Date